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EXAMINER	
WILLIAMS, JEFFERY L	

ART UNIT	PAPER NUMBER
2137	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/051,585	SATO ET AL.	
	Examiner	Art Unit	
	Jeffery Williams	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the communication filed on 10/9/07.

All objections and rejections not set forth below have been withdrawn.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The claim recitations of claims 1, 4, 15, 16 recite:

an interpreter execution program that is configured to generate the command control string from the intermediate code, ***and to decrypt and generate the another command control string from the encrypted intermediate code****, wherein the encrypted intermediate code includes address information indicating where the cipher data for decrypting the encrypted intermediate code is stored within the ROM,* ***the address of the cipher data stored within the ROM being independent of where the encrypted intermediate code is stored in the RAM****; and a* ***CPU configured to judge whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code, independent of where the intermediate code is stored in the RAM****; configured to execute the interpreter execution program for generating the command control string from the intermediate code, and configured to execute* ***the interpreter execution program for decrypting and generating the***

another command control string from the encrypted intermediate code *by accessing the cipher data stored in the ROM at the address identified in the encrypted intermediate code.*

Claims 5 – 9, 11 – 14, and 17 – 19 comprise essentially similar recitations.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1, 4, 12, 13, 15, 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation *"the address identified in the encrypted intermediate code"*, see last line. There is insufficient antecedent basis for this limitation in the claim, as the claim does not recite an address that is identified in the encrypted intermediate code. For the purpose of examination, the examiner presumes the appliant to recite *"an address that is identified in the encrypted intermediate code"*.

Depending claims are rejected by virtue of dependency.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 4 – 9, and 11 – 19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has not pointed out where the new (or amended) claim is supported, nor does there appear to be a written description of the claim limitations in the application as filed (see above objection to the specification).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 12, and 15 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westheimer et al. (Westheimer), "Computer Software Protection System", 4,573,119 in view of Buerkle et al. (Buerkle), "System for Executing Microinstruction Routines By Using Hardware to Calculate Initialization

Parameters Required Therefore Based Upon Processor Status and Control Parameters".

Regarding claim 1, Westheimer discloses:

a RAM configured to store an intermediate code representing a command control string to be executed by a control section and an encrypted intermediate code representing another command control string to be executed by the control section after first being decrypted (Westheimer, fig. 1:48; 2:26-29;4:52-61; claim 8); *and a CPU for controlling execution* (Westheimer, fig. 1:40).

Westheimer discloses a LSI wherein a CPU controls the execution of both encrypted and unencrypted instructions. Westheimer discloses that program instruction or "intermediate code" are fetched by the CPU, wherein an instruction is identified by an opcode and operated upon accordingly. However, Westheimer does not disclose that the CPU operates using an "interpreter execution program" to process the programmed instructions [encrypted or unencrypted], and that such an "interpreter execution program" is stored in a ROM.

Buerkle teaches that LSI processors utilize an "interpreter execution program" [microprogram] to allow a CPU to process intermediate code [macroinstructions] according to the opcodes of the instructions. Buerkle teaches that prior art discloses LSI's as storing the "interpreter execution program" in a ROM (Buerkle, "Description of the Related Art").

It would have been obvious to one of ordinary skill in the art to recognize the need for an "interpreter execution program" stored in a ROM to allow a CPU to control the execution of an "intermediate code", and thus follow the LSI processor design teachings of Buerkle within the LSI processor system of Westheimer. This would have been obvious because one of ordinary skill in the art would have been motivated to practically implement the features known in prior art to be included within LSI processor systems.

the combination furthermore enables:

a ROM configured to store cipher data used for decrypting the encrypted intermediate code, wherein the encrypted intermediate code includes address information indicating where the cipher data for decrypting the encrypted intermediate code is stored within the ROM, the address of the cipher data stored within the ROM being independent of where the encrypted intermediate code is stored in the RAM; (Westheimer, 8:32-45)

a CPU configured to judge whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code, independent of where the intermediate code is stored in the RAM (Westheimer, fig. 1:40; 2:54-57)*; configured to execute the interpreter execution program for generating the command control string from the intermediate code; and configured to execute the interpreter execution program for decrypting and generating the another command control string from the encrypted intermediate code* (Buerkle, "Description of the Related Art") *by accessing the cipher data stored in the ROM at the address identified in the encrypted intermediate*

code (Westheimer, 8:32-45 – herein, Westheimer discloses that encrypted intermediate code comprises several qualities, one of which is an address identifying the cipher data stored in ROM).

Regarding claim 12, the combination enables:

the RAM, the ROM, and the CPU are formed on one chip (Westheimer, 2:26-29).

Regarding claim 15, the combination enables:

wherein the CPU judges whether intermediate code obtained from the RAM is the intermediate code or the encrypted intermediate code based on header information included in the intermediate code (Westheimer, fig. 1:40; 2:54-57).

Regarding claim 16, the combination enables:

wherein the header information is a flag (Westheimer, fig. 1:40; 2:54-57).

Regarding claims 17 – 19, they are substantially similar to claims 1, 12, 15, and 16, and they are rejected, at least, for the same reasons.

Claims 4 – 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Westheimer and Buerkle in view of Hagiwara et al. (Hagiwara) "Disk Drive computer with Programmable Nonvolatile

Memory Capable of Rewriting a Control Program of the Disk Drive", U.S. Patent 6,393,561.

Regarding claim 4, the combination of Westheimer and Buerkle disclose:

the RAM, the ROM, the CPU and the control section are formed on one chip (Westheimer, 2:26-29).

The combination of Westheimer and Buerkle discloses in general a secure and programmable LSI microprocessor wherein executed instructions can be stored in encrypted or decrypted form. The combination does not disclose an optical disk control section and a recording/reproduction head.

Hagiwara teaches that programmable LSI microprocessors can be incorporated with an optical disc device, wherein the control of the disk drive is by customized application programs stored within the programmable LSI microprocessors (Hagiwara, "Technical Field"; 5:13-59; 6:61-7:2; 15:48-53; 13:44-49; 19:30-39). The included programmable LSI microprocessor section of the disk drive controls the optical disk drive in response to requests from a host (Hagiwara, 11:64-67). Hagiwara teaches that programmable LSI microprocessors within optical disk drives beneficially aids the manufacturing cycle of such drives for customers (Hagiwara, 3:57-60; 4:55-67; 6:1-7).

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Hagiwara for combining a optical disk drive with a programmable LSI microprocessor within the secure, programmable LSI microprocessor system of the combination of Westheimer and Buerkle. This would have been obvious, because one

of ordinary skill in the art would have been motivated by the disclosed need within prior art to equip disk drives with programmable LSI microprocessors.

The combination enables an *optical disk control section* (Hagiwara, fig. 1:5) and *a recording/reproduction head* (Hagiwara, fig. 1:11).

Regarding claim 5, it contains essentially similar limitations as claim 4, and it is rejected, at least, for the same reasons. Furthermore, the combination enable an "execution section" (Westheimer, fig. 1:20; Hagiwara, fig. 1:5). The combination enables for the execution of "intermediate code" that is to effect a useful result (Westheimer, 1:14-26), the useful result being for the controlling of the reproduction/recording of information on an optical disk (see rejection of claim 4). Thus the execution results in a "command control string" to control the optical disk drive.

Regarding claim 6, it is rejected, at least, for the same reasons as claim 1.

Regarding claim 7, it is rejected, at least, for the same reasons as claim 4.

Regarding claim 8, the combination enables:

a recording/reproduction head for recording/reproducing information on an optical disc (Hagiwara, fig. 1:11);

an optical disc control section for controlling a motor which drives the optical disc (Hagiwara, fig. 1:10),

wherein the optical disc control section is comprised within the control section (Westheimer, fig. 1:20; Hagiwara, fig. 1:5), *and the RAM, the ROM, the CPU and the control section are formed on one chip* (Westheimer, 2:26-29).

Regarding claim 9, the combination enables:

wherein the optical disc control section is formed on the one chip (Westheimer, 2:26-29).

Regarding claim 11, the combination enables:

the RAM stores the encrypted intermediate code and the unencrypted intermediate code (Westheimer, fig. 1:48; claim 8).

Regarding claim 13, the combination enables:

wherein the intermediate code represents user customized command control strings (Hagiwara, 5:36-42), *and the encrypted intermediate code represents vendor proprietary command control strings* (Westheimer, 1:14-26).

Regarding claim 14, it contains essentially the same limitations as claim 13, and it is rejected, at least, for the same reasons.

Response to Arguments

Applicant's arguments filed 10/9/2007 have been fully considered but they are not persuasive.

Applicants argue or assert primarily that:

(i) Applicants request the withdrawal of the objection to the specification and rejection of the claims under 35 USC §112, 1st par. (Remarks, pg. 7)

In response, the examiner respectfully notes that the claim recitations in question do not appear to be supported by the applicant's original disclosure and the applicant's have failed to point out support for the recitations in question.

(ii) *Accordingly, to the extent the Examiner may consider Westheimer et al. to include address information indicating where the cipher data is stored in the ROM, the address is not independent of where the encrypted data is stored in the RAM as recited in claims 1,5 and 17.* (Remarks, pg. 9)

In response, the examiner respectfully notes that the cipher data and the program code are separately stored, and thus the addresses are independent.

(iii) *The combination of Westheimer and Buerkle does not enable intermediate code and an interpreter execution program stored in ROM. (Remarks, pg. 10- 14).*

In response, the examiner notes that the prior art clearly shows the decoding of program instructions into machine understandable instructions and a means to do so stored in ROM ("interpreter execution program") (i.e. Buerkel, col. 1, 2).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Notice of References Cited.

A shortened statutory period for reply is set to expire **3** months (not less than 90 days) from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffery Williams whose telephone number is (571) 272-7965. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Williams
Art Unit 2137

SUPERVISORY PATENT EXAMINER